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Nonisolated DC-DC Converters with Wide Conversion Range for High-Power Applications

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Abstract—This paper presents the conception of a family of dc-dc converters with wide conversion range (WCR) based on the multi-state switching cell (MSSC) for high-power, high-current applications. The resulting topologies allow achieving high-voltage step-up/step-down in a modular approach, as the WCR-MSSC cell is obtained by using isolated secondary windings coupled to the autotransformer of the MSSC with series-connected controlled rectifiers. Depending on the transformer turns ratio, it is possible to adjust the static gain and reduce the voltage stresses across the main switches, thus allowing the use of metal oxide semiconductor field effect transistors (MOSFETs) with low on-resistance $R_{DS(on)}$, as efficiency is improved as a consequence of minimized conduction losses. A dc-dc boost-type converter based on the four-state switching cell (4SSC) is also implemented, thoroughly analyzed, and evaluated experimentally to demonstrate the advantages associated to the proposed approach in the conception of novel dc-dc converter topologies for this purpose.

Index Terms—dc-dc converters, multi-state switching cell, step-up dc-dc converters, wide conversion range.

I. Introduction

Dc-dc converters play an important role in modern applications when adapting existing voltage and current levels involving distinct types of sources and loads. Renewable energy systems, e.g., solar photovoltaic, fuel cell, and small wind energy conversion ones may depend on low dc voltages (12 Vdc – 48 Vdc) due to the presence of a dc-link composed by filter capacitors or back-up batteries. In practice, many series-connected elements are often undesirable to avoid redundancy, minimize cost, and increase robustness. Low dc voltages are then supposed to be stepped up to levels ranging from 200 Vdc to 800 Vdc to supply cascaded single-phase or three-phase voltage source inverters typically found in off-grid and on-grid systems, submerged water pumps, motor drives, among others [1] [2].

In applications involving wide conversion range (WCR), power converters employing high-frequency transformers are the most obvious choice since the static gain can be adjusted not only according to the duty cycle, but also the turns ratio between the windings. However, it is worth to mention that the transformer leads to the increase of overall size, weight, and volume of the converter in high-power applications [3].

If galvanic isolation is not necessary, it is possible to use nonisolated dc-dc converters instead with consequent reduction of dimensions and increase of efficiency due to the lack of a high-frequency transformer. The classical buck and boost converters are the preliminary choices in voltage step-down and step-up, respectively, mainly due to simplicity, low component count, and reduced stresses if compared with the buck-boost, Ćuk, SEPIC, and Zeta topologies, although some important practical issues must be taken into account. In order to achieve WCR with the aforementioned topologies, extremely low or high duty ratios would be necessary, thus demanding the use of high-cost and complex drivers for this purpose. When using boost-derived converters and high duty ratios, the parasitic resistance regarding the filter inductor also causes appreciable I^2R losses, thus leading to poor efficiency and reduction of the static gain [4].

Literature presents some interesting approaches that allow obtaining WCR in both step-down and step-up nonisolated dc-dc converters. Considering particular advantages and disadvantages addressed to the existing structures, cascaded converters, coupled-inductor-based converters, switched-capacitor-based converters, and converters using voltage multiplier cells (VMCs) can be used in practice.

Perhaps one of the earliest works on the subject is the one introduced in [5], where single-switch topological variations of cascaded dc-dc converters are described. The so-called quadratic converters provide high-voltage step-up or step-down by simply assuming that the overall static gain is equal to the product of the static gains associated to the existing converters. Even though this is a modular solution able to achieve WCR in both cases, the resulting topologies are not viable for high-power applications because energy is processed by multiple cascaded stages, thus compromising the overall efficiency. The appreciable voltage stresses regarding the semiconductor elements are also of major concern.

Coupled inductors are a possible alternative to extend the static gain of dc-dc converters [6]. The leakage inductance can be used to limit the diode current falling rate, thus minimizing the diode reverse-recovery problem. Furthermore, the coupled inductor is employed as a transformer to avoid operation with very high duty ratios and reduce the current ripple in high step-up conversion [7]. For instance, a coupled-inductor-based dc-dc boost converter with low component count is introduced in [8], where the turns ratio allows adjusting the static gain as desired in a simple and straightforward approach. However, the leakage inductance may lead to high voltage spikes, which will increase the voltage stress across the switch causing high electromagnetic interference (EMI) levels and reducing efficiency. The input current is also pulsating, as a low-pass filter may be necessary to further mitigate EMI issues.

Capacitors can be integrated to dc-dc converters by using a switched approach that allows increasing the voltage gain. An example is given in [9], where high-voltage step-up can be achieved by properly increasing the number of capacitors. Since the converter operates typically with low duty cycle, the reverse recovery issue of the output diode is alleviated. The capacitors behave as series-connected voltage sources as the current flows through all of them. Their respective equivalent series resistances must be properly minimized by the parallel association of individual components to achieve a

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given capacitance since they can compromise efficiency. Drive circuitry also becomes more complex as more switches are added, which are not connected to the same reference node. It is also worth to mention that the voltage stresses across them are not the same, leading to the specification of active switches with multiple ratings.

VMCs have been successfully used to obtain novel converter topologies with WCR [10]. A modular and flexible approach results when combining diodes and capacitors as in [11], where a family of nonisolated dc-dc converters is proposed. However, as more VMCs are added, high component count associated to increased conduction and switching losses in the multiplier diodes are possible drawbacks.

Even though there are many other dc-dc converter topologies with high-voltage step-up characteristic, most solutions are only able to process power levels lower than 1 kW, thus motivating the search for topologies able to achieve higher power levels with increased efficiency in [12]. When dealing with high-power, high-current applications, interleaving is one of the most popular and obvious choices as a modular approach, where the output power can be increased by using additional switches, inductors, and diodes. Literature presents some dc-dc interleaved boost converters capable of achieving high-voltage step-up based on VMCs [13], coupled inductors [14], or a combination of both approaches [15]. For instance, a six-phase interleaved double dual boost converter is proposed in [16], whose efficiency is 92.8% at the rated power of 2.2 kW. However, the voltages across the output filter capacitors must be balanced and controlled independently using a proper control scheme. Another important issue that must be taken into account in interleaving topologies lies in the fact that current sharing among the phases can be compromised due to eventual inherent differences regarding the semiconductor elements and inductors, while duty cycle mismatch must also be analyzed in detail [17]. Consequently, balancing the current through the phases may require the use of complex control techniques as described in [18].

Within this context, this work proposes a family of dc-dc converters with WCR adequate for high-power, high-current applications. It consists in a modular approach that allows modifying the static gain while also keeping reduced voltage stresses across the semiconductors, which is essential to minimize conduction losses and achieve high efficiency at high power levels. Thus it is possible to derive unidirectional or bidirectional step-down, step-up, and step-up/step-down dc-dc converter topologies that can be used in a wide range of applications. Since renewable energy conversion systems often require dc-dc converters with high-voltage step-up, a boost-type converter is proposed and thoroughly evaluated so that it is possible to validate the theoretical assumptions. A 3-kW experimental prototype is developed, where it is possible to validate the theoretical assumptions.

II. Generation of Novel Converter Topologies and Proposed High-Voltage Step-Up Boost Converter

The canonical cell or two-state switching cell (2SSC) is part of the basic dc-dc converter topologies, being composed by one active switch and one diode that operate complementarily [19, 20]. This arrangement can also be represented using the pulse width modulation (PWM) switch model for the small-signal analysis in terms of a three-terminal element [21, 22]. Bidirectional converters can also be obtained if the diode is simply replaced by an active switch.

The load power in the aforementioned topologies is processed by a single semiconductor in each operating stage, as such structures present inherent limitation when power levels come to increase. The 2SSC can then be replaced by the multi-state switching cell (MSSC), which is composed by several 2SSCs connected to each other by an autotransformer to achieve higher current levels, as the number of switching states can be increased as associated to additional semiconductors [23]. A bidirectional version of the MSSC is shown in Fig. 1 (a), which employs one autotransformer with multiple windings connected to the legs composed by lower-side active switches S_1, S_2,…, S_n and upper-side active switches S_1', S_2',…,S_n'. It is also worth to mention that a unidirectional version can be obtained by replacing the upper-side active switches for diodes. The autotransformer in this case plays a key role in providing good current sharing among the several legs constituted by semiconductors considering that all windings have the same number of turns.

Depending on the number of switching states N assumed by the MSSC, there are N-1 possible operating regions, while the gating signals that drive the active switches must be phase-shifted by 360°/(N-1) analogously to interleaving. However, if the autotransformer presents unity turns ratio, it is possible to achieve high power levels in a modular approach with good current sharing without the need of special control schemes. Other prominent advantages addressed to the MSSC are reduced current stresses through semiconductors, with minimized conduction losses when metal oxide semiconductor field effect transistors (MOSFETs) are employed; consequent increase of overall efficiency; improved utilization of heat sinks with proper distribution of losses; reduced dimensions and weight of filter elements, which are designed for a multiple of the switching frequency.

If the 2SSC that exists in the six classical dc-dc converters is simply replaced by the bidirectional version of the MSSC shown in Fig. 1 (a), the very same static gain is obtained considering the operation in continuous conduction mode (CCM). In order to obtain dc-dc converters with WCR, several additional secondary windings can be coupled to the windings of the autotransformer of the MSSC and associated to series-connected active rectifiers as seen in Fig. 1 (b), as the resulting arrangement is called WCR-MSSC. It is able to provide unidirectional or bidirectional power flow, also allowing the increase of power levels and/or the conversion ratio as desired. It is also worth to mention that the autotransformer becomes a multi-phase transformer since the secondary windings are coupled to the primary ones, which formerly belong to the MSSC.

The canonical cell is a three-port element that exists in the classical dc-dc converters, been represented by terminals a, b, and c in the conventional buck, boost, buck-boost, Ćuk, single-ended primary inductance converter (SEPIC), and Zeta topologies in Fig. 2. Although only their respective bidirectional versions are shown in a more generic representation, it can be stated that unidirectional converters can be promptly obtained when substituting switch S_1' for a diode. This switching cell can then be simply replaced by the proposed WCR-MSSC shown in Fig. 1 (b), resulting in a family of bidirectional converters for high-voltage step-up and/or step-down as shown in Fig. 2. The lower-side active switches S_1, S_2,…, S_n and upper-side active switches S_1', S_2',…,S_n' are part of the MSSC. On the other hand, S_{ajn} and

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S_{ajn}' denote active switches that are part of a given controlled rectifier bridge j, being n the total number of phases of the transformer. Besides, unidirectional converters can be obtained substituting S_1', S_2',…, S_n', S_{ajn}, and S_{ajn}' for diodes.

The so-called WCR-MSSC dc-dc converters can be employed in distinct high-power applications, e.g., solar photovoltaic systems [24]. The following advantages can then be addressed to the resulting structures: reduced current stresses regarding the semiconductor elements, since the total current is shared among several legs; reduced voltage stresses across the active switches if compared with the conventional dc-dc converters; inherent modularity; possibility to achieve unidirectional or bidirectional power flow; distinct configurations such as wye or polygon connection can be employed in the secondary side of the multi-phase transformer.

Considering that nonisolated dc-dc converters for high-voltage step-up applications are a modern trend in power electronics, the unidirectional boost converter employing the four-state switching cell (4SSC) shown in

Fig. **3** is presented and analyzed in detail to demonstrate the claimed advantages. It is composed by an input voltage source V_{IN}; a filter inductor L_1; a three-phase Y-Y (wye-wye) transformer with turns ratio $n=N_s/N_p$; active switches S_1, S_2, and S_3; rectifier diodes $D_1…D_9$; auxiliary clamping capacitors C_1 and C_2; an output filter capacitor C_o; and a load resistor R_o.

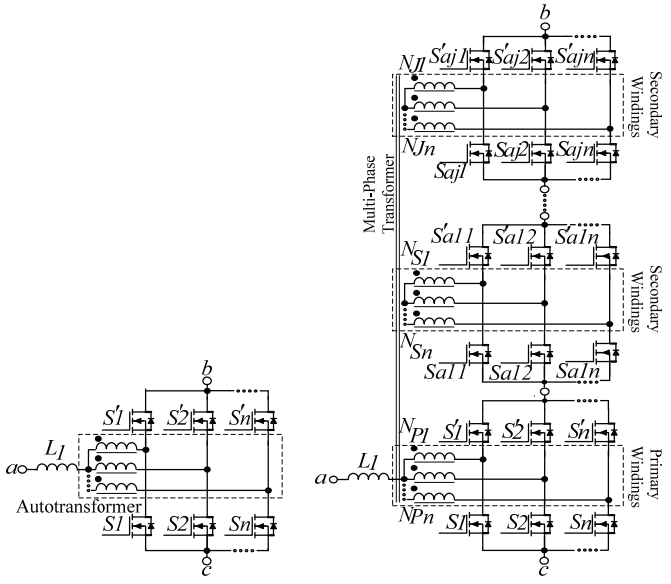

Fig. 1. (a) Bidirectional versions of the (a) MSSC; (b) WCR-MSSC cell.

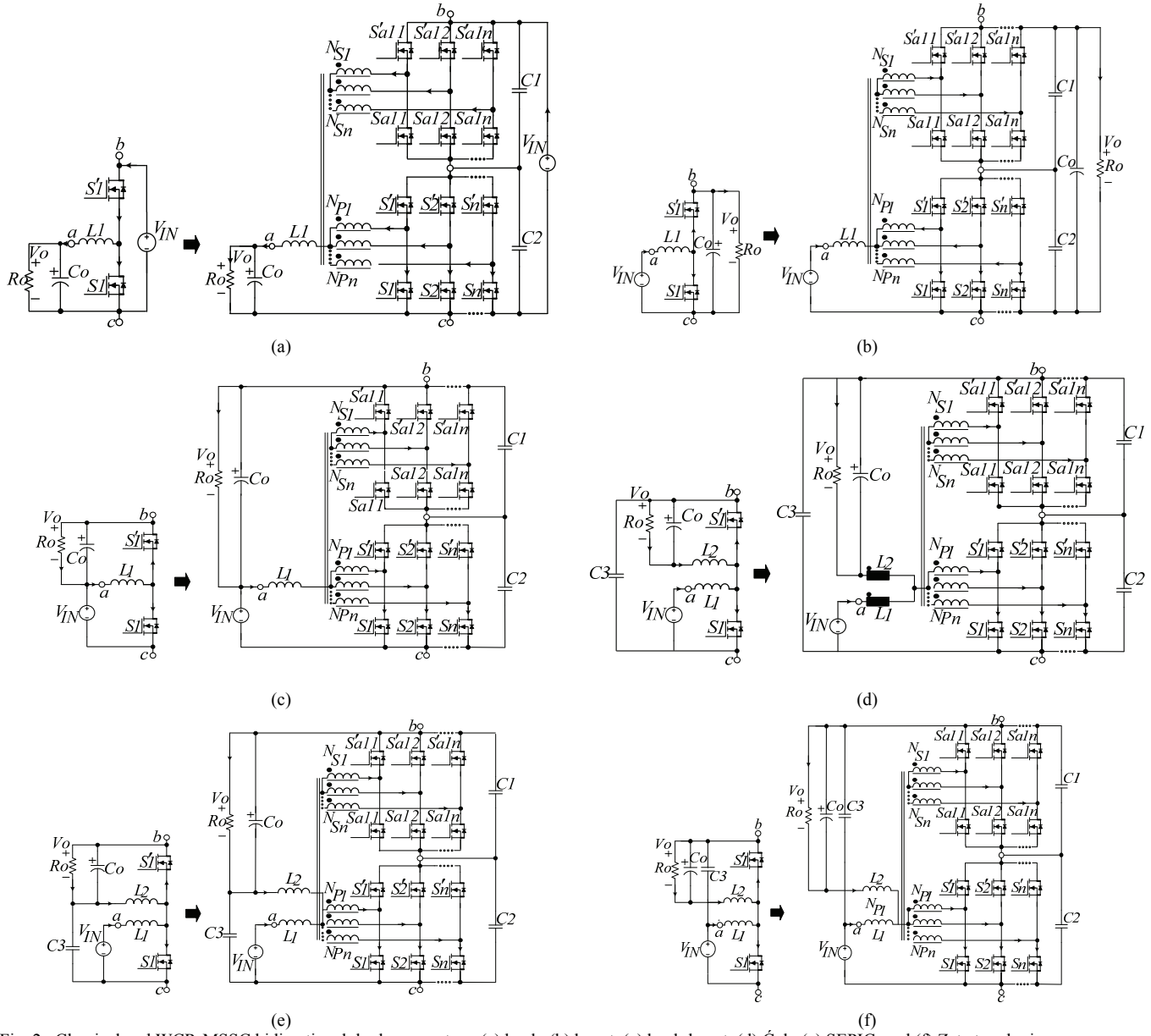

Fig. 2. Classical and WCR-MSSC bidirectional dc-dc converters; (a) buck, (b) boost, (c) buck-boost, (d) Ćuk, (e) SEPIC, and (f) Zeta topologies.

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Since the 4SSC is used in this case, the gating signals of switches S_1, S_2, and S_3 must be phase-shifted by [360°/(4-1)]=120°. Besides, three operating regions exist: R1 ($0<D<1/3$), where a single active switch is on in a given operating stage; R2 ($1/3<D<2/3$), where up to two active switches are on simultaneously in a given operating stage; and R3 ($2/3<D<1$), where up to three active switches are on simultaneously in a given operating stage. It is worth to mention that a same converter presents distinct operating stages for each one of them considering the switching states shown in Table I, thus leading to particularly different qualitative and quantitative analyses.

Applying the volt-second balance to the boost converter operating in CCM for each one of the aforementioned regions, the static gain plots in

Fig. 4 can be obtained. It can be seen that it is not possible to achieve high-voltage step-up in region R1 since the voltage induced in the secondary windings is somewhat low, unless if high turns ratio is adopted. On the other hand, region R3 provides WCR, although extreme duty ratios should be avoided in practice to avoid appreciable I^2R loss due to parasitic resistance of the filter inductor [25]. This is the main reason why the analysis carried out in this work is restricted to region R2 so that it is possible to develop an experimental prototype.

TABLE I
SWITCHING STATES OF THE PROPOSED 4SSC-BASED BOOST CONVERTER IN CCM

Operating Stage	Switching States (S_1, S_2, S_3)		
	R1	R2	R3
1	ON, OFF, OFF	OFF, ON, ON	ON, ON, ON
2	OFF, OFF, OFF	OFF, OFF, ON	OFF, ON, ON
3	OFF, ON, OFF	ON, OFF, ON	ON, ON, ON
4	OFF, OFF, OFF	ON, OFF, OFF	ON, OFF, ON
5	OFF, OFF, ON	ON, ON, OFF	ON, ON, ON
6	OFF, OFF, OFF	OFF, ON, OFF	ON, ON, OFF

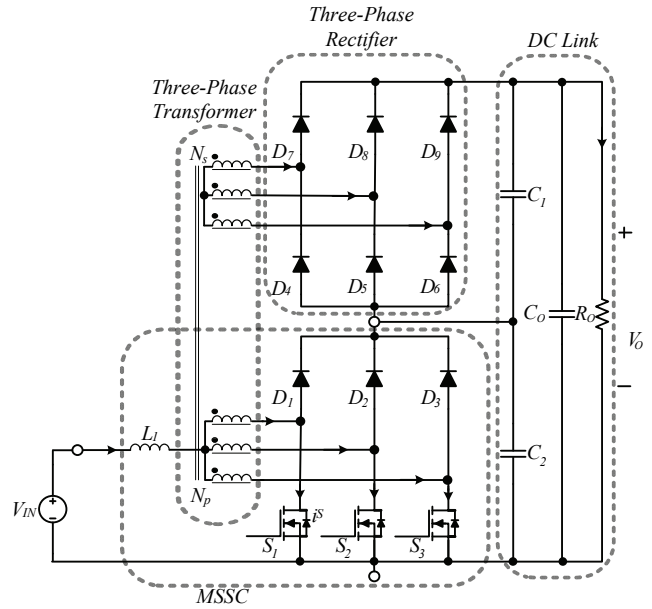

Fig. 3. High-voltage step-up dc-dc boost converter based on the WCR-4SSC.

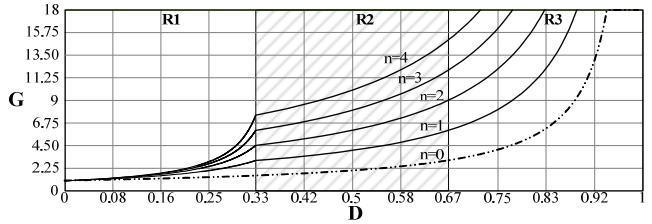

Fig. 4. Static gain of the 4SSC-based boost converter in CCM for distinct turns ratio as a function of the duty cycle.

III. QUALITATIVE ANALYSIS

Considering that the converter operates in region R2 ($1/3<D<2/3$) under CCM and steady-state conditions, six stages result during one switching period T_s as shown in Fig. 5, while the theoretical waveforms are represented in Fig. 6.

First stage [t_0, t_1] (Fig. 5 (a)): Switch S_3 is turned on, while switches S_1 and S_2 keep their previous states and remain off and on, respectively. The current through L_1 increases linearly, flowing through winding T_{p2} and S_2, and also through winding T_{p3} and S_3, as good current sharing is maintained considering that the number of turns is the same for all primary windings. Besides, part of the energy through T_{p1} is directly transferred from the input source to the load. Diodes D_2, D_3, D_4, D_8, and D_9 are reverse biased, while diodes D_1, D_5, D_6, and D_7 are forward biased. This stage finishes when S_2 is turned off.

The voltage across L_1 is given by:

$$V_{L1} = V_{IN} - \frac{V_{C1}}{3} \tag{1}$$

where V_{C1} is the average voltage across capacitor C_1.

The time interval that defines this stage is:

$$t_0 - t_1 = \frac{(3D-1)T_s}{3} \tag{2}$$

Second stage [t_1, t_2] (Fig. 5 (b)): Switch S_2 is turned off, while switches S_1 and S_3 keep their previous states and remain off and on, respectively. The energy stored in L_1 is transferred to C_1 and C_2 and the load, as the inductor current decreases linearly flowing through the primary windings. The inductor voltage polarity is reversed so that the magnetic flux is constant, as the voltages across S_2 and C_1 are equal. Besides, diodes D_3, D_4, D_5, and D_9 remain reverse biased, while D_1, D_2, D_6, D_7, and D_8 are forward biased.

The voltage across L_1 is given by:

$$V_{L1} = V_{IN} - \frac{2V_{C1}}{3} \tag{3}$$

The time interval that defines this stage is:

$$t_1 - t_2 = \frac{(2-3D)T_s}{3} \tag{4}$$

Third stage [t_2, t_3] (Fig. 5 (c)): Due to the inherent symmetry, this stage is analogous to the first one, although switch S_1 is turned on instead, while switches S_2 and S_3 keep their previous states and remain off and on, respectively. Diodes D_1, D_3, D_5, D_7, and D_9 are reverse biased, while diodes D_2, D_4, D_6, and D_8 are forward biased.

Fourth stage [t_3, t_4] (Fig. 5 (d)): This stage is similar to the second one, but switch S_3 is turned off and only S_1 remains on. The energy stored in L_1 is delivered to the load, auxiliary capacitors C_1 and C_2, and output filter capacitor C_o. Diodes D_2, D_3, D_4, D_8, and D_9 are forward biased due to the polarity of the voltage across the transformer windings.

Fifth stage [t_4, t_5] (Fig. 5 (e)): This stage is analogous to the first and third ones, but switch S_2 is turned on, while switches S_1 and S_3 keep their previous states and remain on and off, respectively. The current through L_1 increases linearly. Diodes D_1, D_2, D_6, D_7, and D_8 are reverse biased.

Sixth stage [t_5, t_6] (Fig. 5 (f)): Switch S_1 is turned off, while switches S_2 and S_3 keep their previous states and remain on and off, respectively. Diodes D_1, D_3, D_5, D_7, and D_9 are forward biased due to the polarity of the voltage across the secondary windings. Inductor L_1 provides energy to the load and capacitors C_1, C_2, and C_o. This stage finishes when S_3 is turned on once again as another switching cycle begins.

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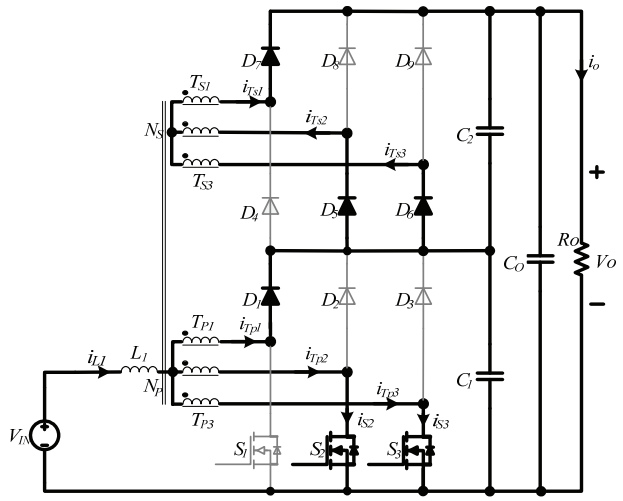
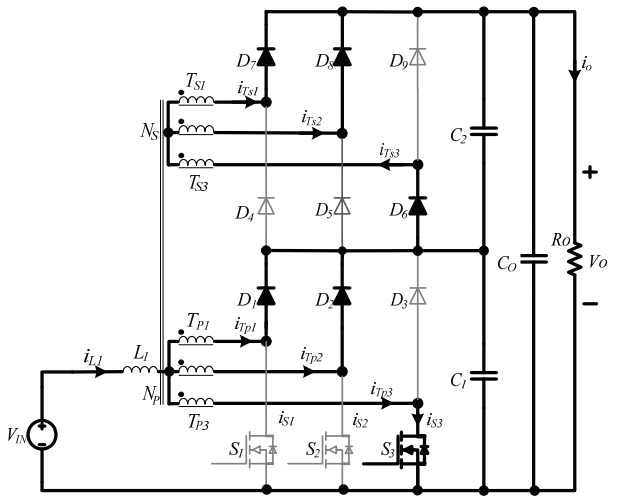
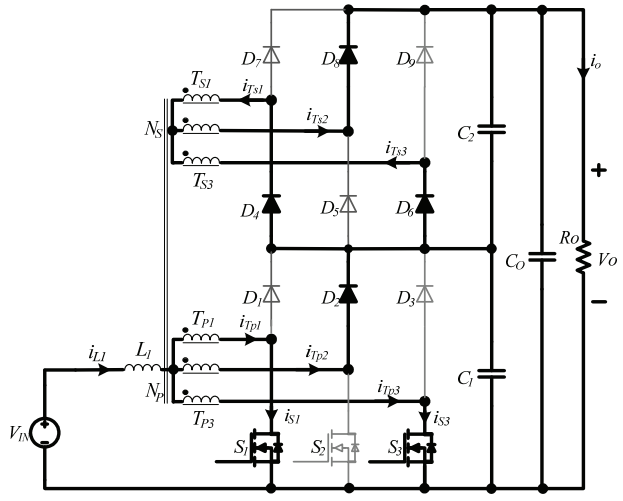


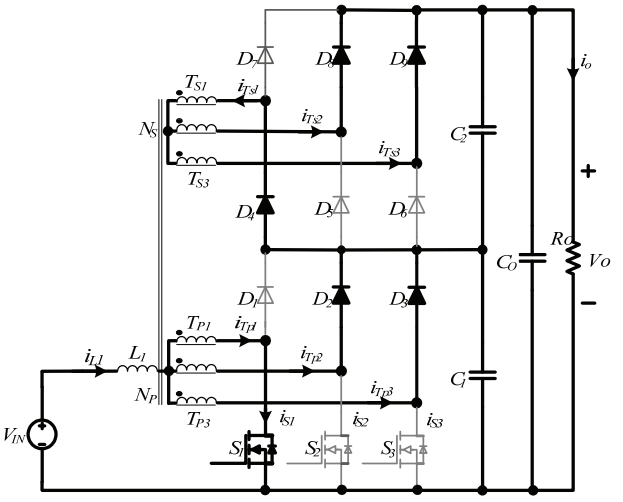
(a) First stage



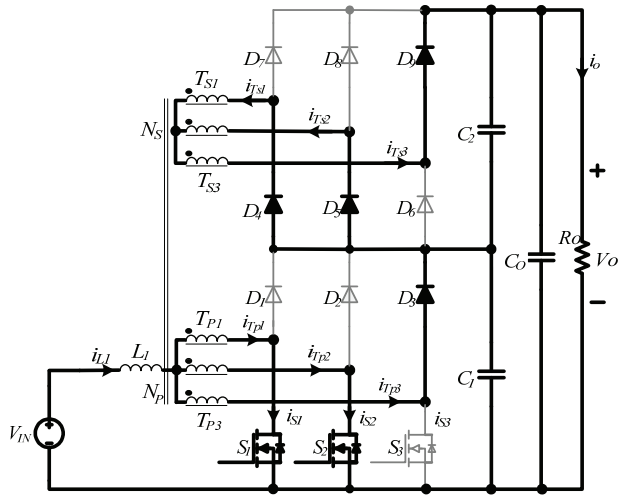
(b) Second stage



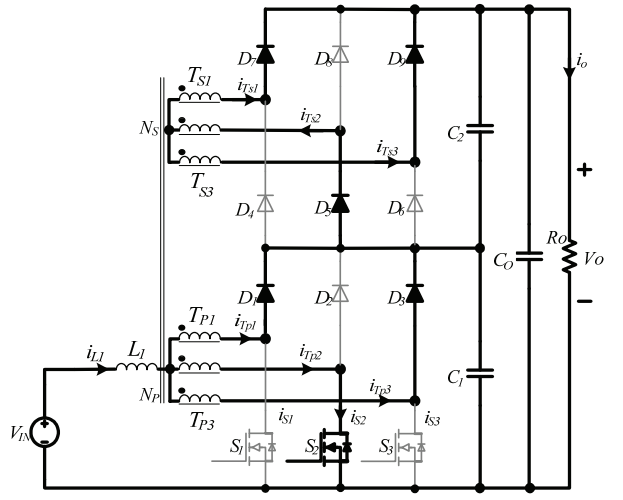
(c) Third stage



(d) Fourth stage



(e) Fifth stage



(f) Sixth stage

Fig. 5. Operating stages of the proposed dc-dc converter.

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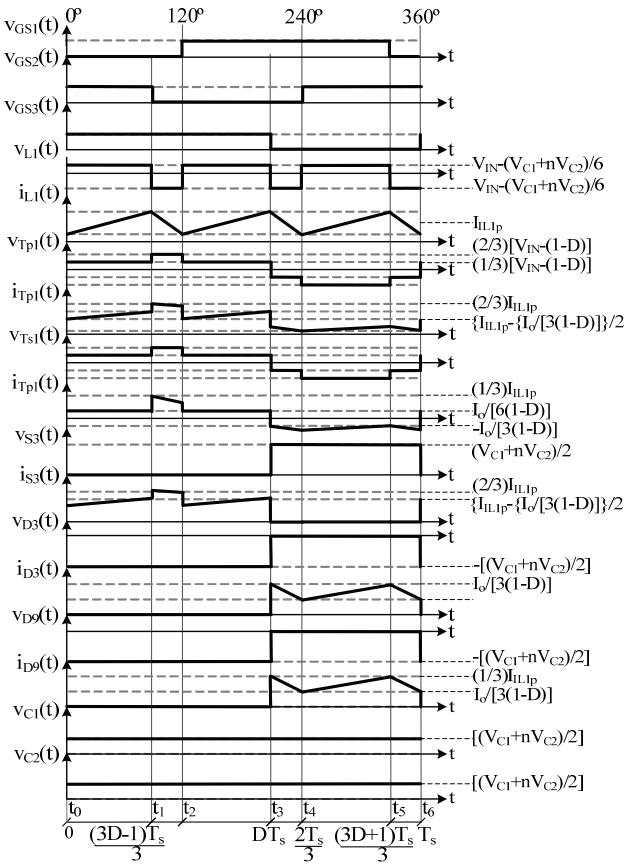

Fig. 6. Main theoretical waveforms.

IV. Quantitative Analysis

A. Static Gain

From the analysis of the equivalent circuits and theoretical waveforms that describe the converter operation in CCM and region R2 as shown in Fig. 5 and Fig. 6, respectively, applying the volt-second balance to filter inductor L_1 gives the static gain as:

$$G = \frac{V_o}{V_{IN}} = \frac{n+1}{1-D}, \text{ if } 1/3 < D < 2/3 \tag{5}$$

The average voltages across capacitors C_1 and C_2 can be also be determined as:

$$V_{C1} = \frac{V_{IN}}{1-D}, \text{ if } 1/3 < D < 2/3 \tag{6}$$

$$V_{C2} = \frac{n \cdot V_{IN}}{1-D}, \text{ if } 1/3 < D < 2/3 \tag{7}$$

If a similar analysis is performed for regions R1 and R3, their respective static gains can be determined as in (8) and (9).

$$G = \frac{V_o}{V_{IN}} = \frac{n+1}{1-D+n\cdot(1-3\cdot D)}, \text{ if } 0 < D < 1/3 \tag{8}$$

$$G = \frac{V_o}{V_{IN}} = \frac{n+1}{1-D}, \text{ if } 2/3 < D < 1 \tag{9}$$

If n=0 in (5), (8), and (9), the static gain is the same as that regarding the classical dc-dc boost converter, which is not able to provide high-voltage step-up in practice. However, the proposed topology allows achieving WCR as the number of turns involving the three-phase transformer increases.

B. Filter Inductor

The average and rms currents through the filter inductor are equal to the input current I_{IN}, i.e.:

$$I_{L1(avg)} = I_{L1(rms)} = I_{IN} = \frac{P_o}{\eta V_{IN}} = \frac{I_o(1+n)}{\eta(1-D)} \tag{10}$$

where η is the expected theoretical efficiency of the dc-dc converter, P_o is the output power, and I_o is the average output current.

The inductor current ripple ΔI_{L1} can be obtained applying Kirchhoff's voltage law to Fig. 5 (a). Substituting (2) in (1) gives (11), which also allows obtaining the input filter inductance. On the other hand, the normalized current ripple $\overline{\Delta I_{L1}}$ is given by (12) and plotted in Fig. 7, where it can be seen that the maximum value occurs at D=0.5.

$$\Delta I_{L1} = \frac{\left(\frac{2}{3} - D\right)(3\mathrm{D}-1)}{3 f_s L_1 (n+1)} V_o \tag{11}$$

$$\overline{\Delta I_{L1}} = \frac{9 f_s \Delta I_{L1} L_1 (n+1)}{V_o} = (2-3D)(3\mathrm{D}-1) \tag{12}$$

where f_s is the switching frequency and V_o is the average output voltage.

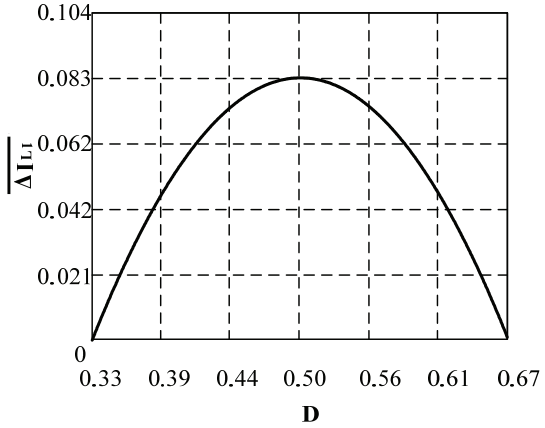

Fig. 7. Normalized current ripple as a function of the duty cycle.

C. Three-Phase Transformer

The rms voltages across the primary and secondary windings are given by (13) and (14), respectively.

$$V_{Tp(rms)} = \frac{\sqrt{6} D V_o}{6} \tag{13}$$

$$V_{Ts(rms)} = \frac{\sqrt{6} n D V_o}{6} \tag{14}$$

The rms currents through each primary and secondary winding are given by (15) and (16), respectively.

$$I_{Tp(rms)} = \frac{I_o(1+n)\sqrt{6(5-3D)}}{12(1-D)} \tag{15}$$

$$I_{Ts(rms)} = \frac{I_o\sqrt{2(7-9D)}}{6(1-D)} \tag{16}$$

The apparent power processed by the transformer is calculated by (17):

$$S_T = \frac{S_o}{\eta_T} = \frac{3 V_{Tp(rms)} I_{Tp(rms)}}{\eta_T} \tag{17}$$

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where S_o is the output apparent power of the dc-dc converter and η_T is the transformer efficiency.

The average and rms currents through active switches $S_1 \ldots S_3$ are given by (18) and (19), respectively, while the maximum voltage across them can be obtained in (20).

$$I_{S(avg)} = \frac{I_o(1+n)(1+D)}{6(1-D)} \tag{18}$$

$$I_{S(rms)} = \frac{I_o\left(1+n\right)\sqrt{26-14D}}{12\left(1-D\right)} \tag{19}$$

$$V_{S(\max)} = \frac{V_{IN}}{1-D} \tag{20}$$

D. Diodes

The average and rms currents through diodes $D_1 \ldots D_3$ and $D_7 \ldots D_9$ are given by (21) and (22), while the maximum reverse voltages across $D_1 \ldots D_3$ and $D_7 \ldots D_9$ can be obtained in (23) and (24), respectively.

$$I_{D1\ldots D3(avg)} = I_{D4\ldots D6(avg)} = I_{D7\ldots D9(avg)} = \frac{I_o}{3} \tag{21}$$

$$I_{D1\ldots D3(rms)} = I_{D7\ldots D9(rms)} = \frac{I_o}{3}\sqrt{\frac{1}{1-D}} \tag{22}$$

$$V_{D1\ldots D3(\max)} = -\frac{V_{IN}}{1-D} \tag{23}$$

$$V_{D4\ldots D6(\max)} = V_{D7\ldots D9(\max)} = -\frac{nV_{IN}}{1-D} \tag{24}$$

The average current through diodes $D_4 \ldots D_6$ can be calculated from (21), while the rms current through them is given by (25). The maximum reverse voltage across them is also obtained from (24).

$$I_{D4\ldots D6(rms)} = \frac{I_o\sqrt{10-14D}}{6\left(1-D\right)} \tag{25}$$

E. Output Filter Capacitor

The output filter capacitor can be calculated according to (26).

$$C_o = \frac{I_o\left(\frac{2}{3}-D\right)\left[3D+\left(1+n\right)-3\right]}{3(1-D)\cdot\Delta V_o\cdot f_s} \tag{26}$$

V. Comparison with Other Nonisolated Dc-Dc Boost-Type Converters for High-Voltage Step-Up

Literature presents numerous topologies that provide high-voltage step-up based on the boost converter for distinct purposes. Research effort is often focused on extending the conversion ratio, reducing component count and consequently size, weight, and volume, minimizing the stresses regarding the semiconductor elements, and also increasing efficiency. Unfortunately, most solutions are only feasible to low-power practical applications typically rated at a few hundred watts.

Interleaving is possibly the most common solution for high-power, high-current applications. An interleaved boost converter based on coupled inductors is proposed in [26] to achieve reduced current ripple and increase the static gain if compared with the conventional boost topology. Even though zero reverse-recovery of the output diodes exists, the structure is only able to operate with $0<D<0.5$. Besides, the static gain depends solely on the duty cycle.

An interleaved boost converter employing coupled inductors in a cross-winding configuration is analyzed in [27], where it is possible to further extend the conversion range as the turns ratio is increased. Low component count and reduced stresses on the active switches can be addressed as prominent advantages. However, the leakage inductance causes some voltage ringing in the active switch and efficiency may not be satisfactory at high power levels. The converter only operates adequately for duty ratios higher than 0.5.

It is worth to mention that the 4SSC-based boost converter in this case consists of a three-phase (or three-cell) arrangement unlike the topologies in [26, 27], and consequently higher component count will result as three active switches are employed. On the other hand, it presents the lowest total device rating (TDR) among the analyzed topologies, being also able to achieve good current sharing without special control schemes if the transformer is adequately implemented in practice. Significant reduction of filter elements is also obtained in this case, as it is possible to use only film capacitors even at high power levels, which is desirable since longer useful life results. On the other hand, the interleaved converters presented in [26, 27] depend strongly on the use of electrolytic capacitors.

TABLE II
COMPARISON AMONG THE PROPOSED CONVERTER AND OTHER SIMILAR APPROACHES

Parameter	[26]	[27]	Proposed Converter
Static gain	$\frac{1}{1-2D}$	$\frac{n}{1-D}$	$\frac{n+1}{1-D}$
Voltage stress on the switches	$\left(\frac{1-D}{1-2D}\right)V_o$	$\frac{V_o}{n}$	$\frac{V_o}{n+1}$
Active switches	2	2	3
Diodes	2	2	9
Magnetically-coupled elements	Coupled inductors	Coupled inductors	Transformer coupled windings
Total number of windings	2	6	6
Total number of magnetic cores	1	2	2
Capacitors	1	1	3
TDR	$\frac{2P_o}{1-2D}$	$\frac{4P_o}{1-D}$	$\frac{2P_o}{1-D}$
Modularity	Yes	No	Yes
Duty cycle limitation	Yes	Yes	No

VI. Experimental Results

From the theoretical analysis carried out in the previous sections, it is possible to design the dc-dc boost converter based on the 4SSC shown in

Fig. 3 properly, whose specifications are listed in Table III. The mathematical expressions provided in Section IV have then been used to implement the experimental prototype represented in Fig. 8, which employs the components described in Table IV. It is worth to mention that the prototype was implemented considering the local availability of components in the laboratory, especially in terms of a dc voltage source capable of providing high input currents.

Firstly, the theoretical static gain curve of the dc-dc converter operating with $1/3<D<2/3$ is compared with the one obtained experimentally in Fig. 9. The leakage inductance of the transformer, which is typically small and rated at L_{lkg}=1.3 μH in this case, does not influence the conversion ratio significantly. The main difference between the curves for n=1

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is due to the intrinsic series resistance of the filter inductor, which tends to influence the behavior of boost-type topologies strongly in practice [28].

Fig. 10 shows the drive signal applied to active switch S_1 and also the inductor current, thus demonstrating that the converter operates in CCM. It can be seen that the current ripple frequency is three times the switching frequency, as the dimensions of filter elements are consequently reduced.

The voltages across the auxiliary capacitors are represented in Fig. 11, which are properly balanced and equal to about 200 V. It is worth to mention that their sum corresponds to the output voltage, i.e., 400 V. Since the voltage ripple frequency is three times the switching frequency when the 4SSC is employed, it is possible to reduce the required filter capacitances, thus avoiding the use of electrolytic capacitors and consequently increasing the useful life of the converter.

TABLE III
DESIGN SPECIFICATIONS

Parameter	Value
Minimum input voltage	V_{IN}=86 V
Output voltage	V_o=400 V
Inductor current ripple	ΔI_L=15%·$I_{L(avg)}$
Output voltage ripple	ΔV_o=1%·V_o
Rated duty cycle	D=0.57
Switching frequency	f_s=35 kHz
Rated output power	P_o=3 kW
Converter efficiency	η=96%
Transformer turns ratio	n=1

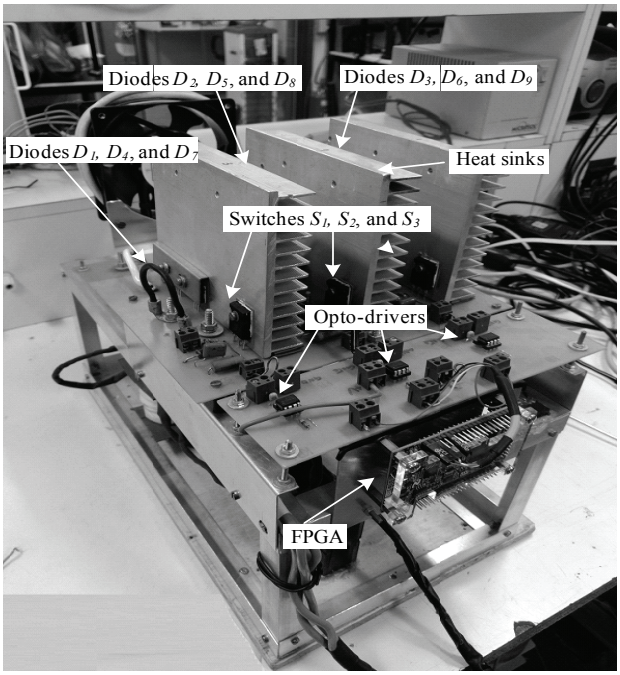

Fig. 8. Experimental prototype.

TABLE IV
POWER STAGE ELEMENTS

Parameter	Value
Filter inductor	L_1=29.12 µH, 11 turns, 24×21 AWG, core E-65/33/26 – IP6
Y-Y three-phase transformer	N_p=8, N_s=8, 9×21 AWG, two cores NC 100/57/25 – IP6 and one core NI-100/24/25 – IP6
Main switches S_1…S_3	MOSFET IRFP4768PbF
Diodes D_1… D_9	30CPH03
Auxiliary capacitors C_1, C_2	220 nF/630 V – polyester capacitors
Output filter capacitor C_o	2×2.2 µF/500 V – polypropylene capacitors

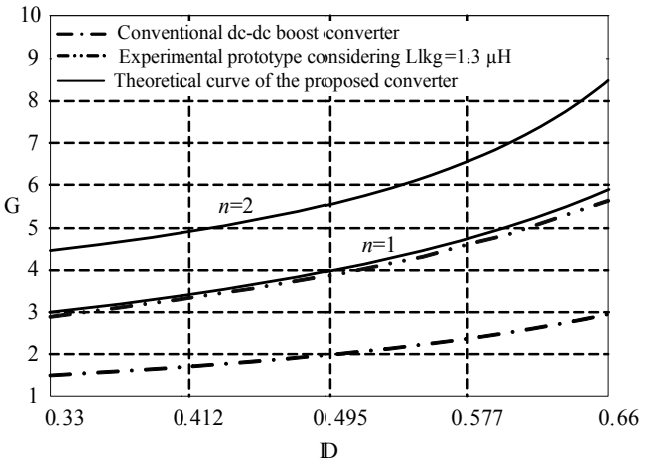

Fig. 9. Comparison among static gain curves.

The current and voltage waveforms in the primary and secondary windings are shown in Fig. 12 and Fig. 13. The currents through the windings are slightly different than the theoretical waveforms due to the leakage inductance, which assumes a low value and does not influence the converter operation significantly. Good current sharing is also achieved when analyzing the currents through the primary windings in Fig. 14, which are phase-shifted by 120°.

Fig. 15 corresponds to the current and voltage waveforms in S_1, considering that the rated duty cycle is about 0.57. According to Fig. 16, the maximum reverse voltage across D_7 is close to 200 V. Besides, it can be seen that the current waveform is associated to the negative half cycle of the current through the secondary winding.

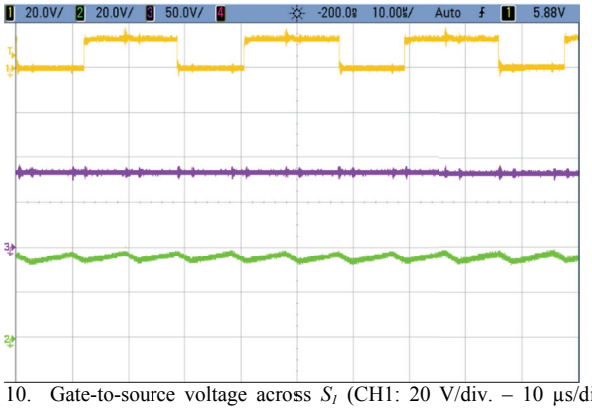

Fig. 10. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.), input voltage (CH3: 50 V/div. – 10 µs/div.), and inductor current (CH2: 20 A/div. – 10 µs/div.).

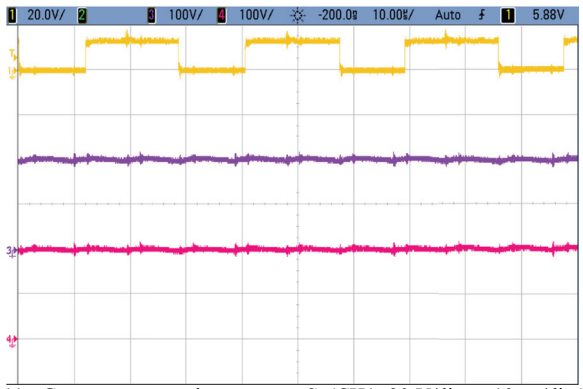

Fig. 11. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.) and voltages across C_1 (CH3: 100 V/div. – 10 µs/div.) and C_2 (CH4: 100 V/div. – 10 µs/div.).

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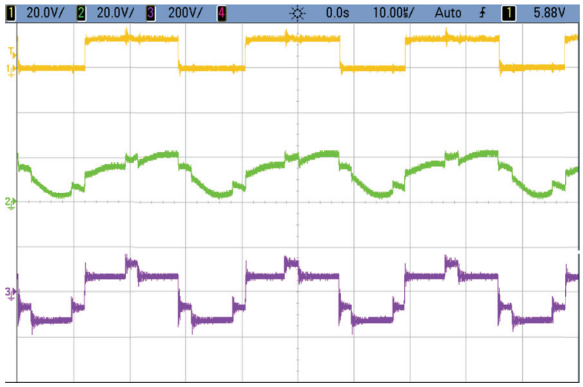

Fig. 12. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.), voltage across the primary winding (CH3: 200 V/div. – 10 µs/div.) and current through the primary winding (CH2: 20 A/div. – 10 µs/div.).

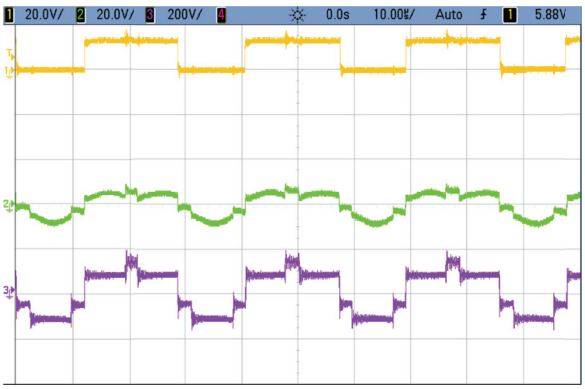

Fig. 13. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.), voltage across the secondary winding (CH3: 200 V/div. – 10 µs/div.) and current through the secondary winding (CH2: 20 A/div. – 10 µs/div.).

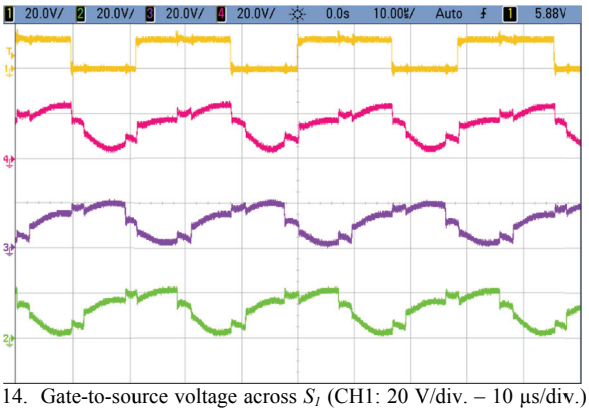

Fig. 14. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.) and currents through the primary windings (CH2, CH3, CH4: 20 A/div. – 10 µs/div.).

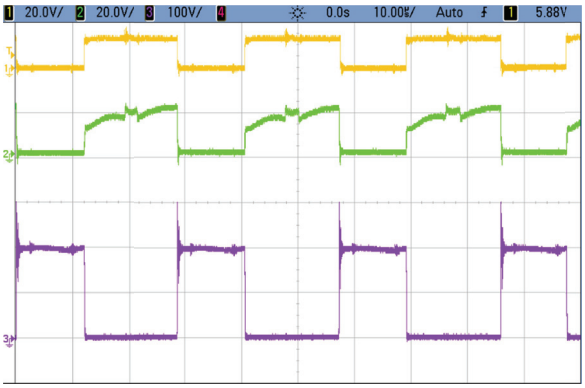

Fig. 15. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.), drain-to-source voltage across S_1 (CH3: 100 V/div. – 10 µs/div.) and current through S_1 (CH2: 20 A/div. – 10 µs/div.).

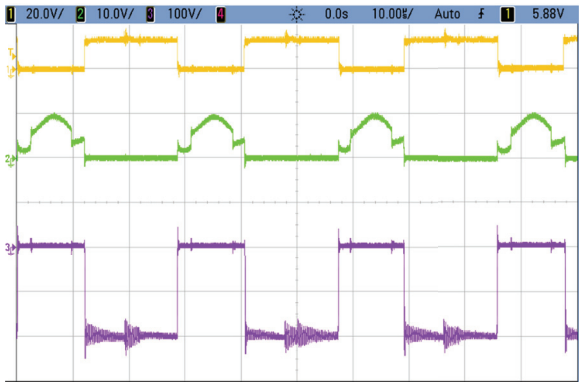

Fig. 16. Gate-to-source voltage across S_1 (CH1: 20 V/div. – 10 µs/div.), voltage across diode D_7 (CH3: 100 V/div. – 10 µs/div.) and current through diode D_7 (CH2: 10 A/div. – 10 µs/div.).

The loss profile is given in Fig. 17, where it can be seen that losses are mainly due to diodes considering that nine passive semiconductors are required in this case according to Fig. 3. The efficiency curve is shown in Fig. 18, where the output power varies from 10% to 100% of the rated load condition. Efficiency is about 96% at 3 kW, thus demonstrating that the converter is adequate for high-power applications where WCR is necessary.

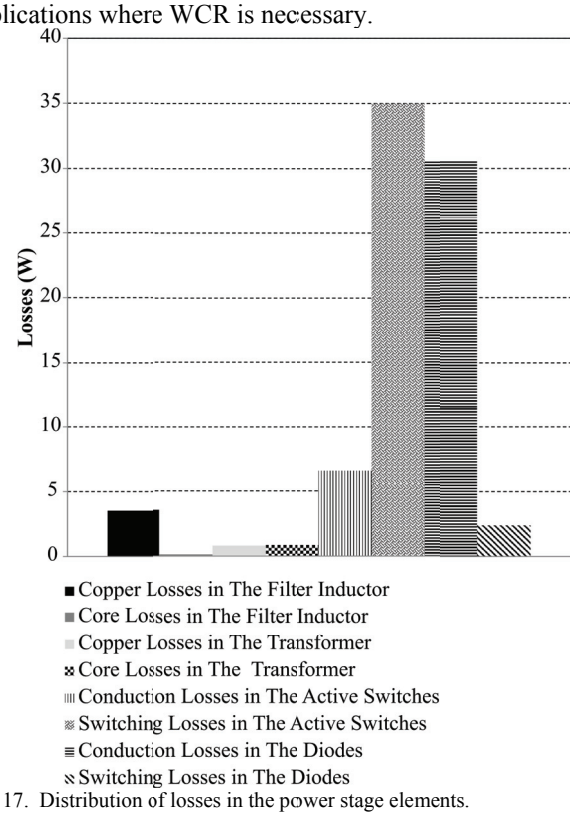

Fig. 17. Distribution of losses in the power stage elements.

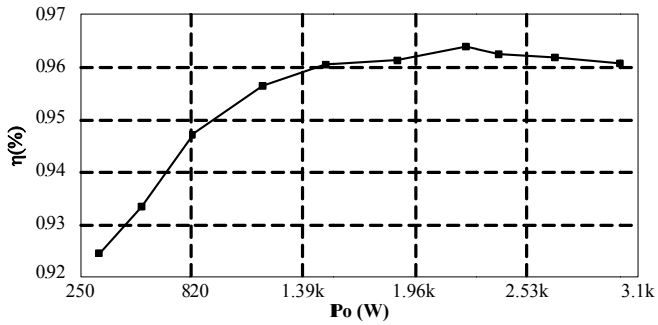

Fig. 18. Efficiency as a function of the output power.

VII. Conclusion

This paper has presented the conception of nonisolated dc-dc converters with WCR based on the MSSC, which are

adequate for high-power, high-current applications. The proposed approach can be considered as an extension of the canonical cell so that higher power levels can be achieved in a modular approach. It is then possible to add more phases to the transformer and also legs composed by semiconductors to achieve unidirectional or bidirectional power flow as desired.

A high-voltage step-up dc-dc boost converter based on the 4SSC has been thoroughly studied to demonstrate its proper advantages. Considering that the current and voltage ripple frequencies associated to filter elements are equal to a multiple of the switching frequency, reduced dimensions of filter elements result. Besides, the current is properly shared among the semiconductors since the transformer windings present nearly the same impedance, thus allowing better heat distribution and reduced current stresses.

Distinct configurations can be adopted for the three-phase transformer, i.e., wye-wye or wye-delta, which can be extended to a polygon connection in the case of a multi-phase structure.

Unlike interleaving, energy is supplied from the input voltage source to the load through the transformer windings while the inductor current increases linearly, thus implying improved performance in terms of overall efficiency. It is then expected that the very same advantages can be obtained in the conception of other converter topologies based on the WCR-MSSC.

High component count could be considered as a possible drawback, but good tradeoffs can be obtained by adjusting the design parameters properly such as the number of phases and transformer turns ratio.

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